DESIGN AND ANALYSIS OF A FAULT-RESILIENT 12T SRAM FOR SPACEBORNE CMOS SYSTEMS

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***Abstract*—** The increasing demand for reliable, low-power memory in aerospace and satellite applications has necessitated the development of robust SRAM designs capable of withstanding harsh radiation environments. This paper presents the design and analysis of a fault-resilient 12-transistor (12T) Static Random Access Memory (SRAM) cell implemented using nanoscale CMOS technology, specifically optimized for Single Event Upset (SEU) tolerance and noise immunity in spaceborne systems. Compared to conventional 6T SRAM designs, the proposed 12T cell offers enhanced read stability, write margin, and soft error resilience without significant trade-offs in power or area at sub-45nm technology nodes. The cell was simulated using industry-standard CAD tools under varying radiation and supply conditions to assess its reliability and performance metrics. The results demonstrate that the 12T SRAM design provides high fault tolerance, making it a suitable candidate for aerospace-grade embedded memory systems.

I. Introduction

Aerospace electronics operate in some of the most extreme and unforgiving environments, where high-energy cosmic particles and ionizing radiation can cause unpredictable failures in integrated circuits. Among the most vulnerable components are SRAM (Static Random Access Memory) cells, which are essential for data storage and cache memory in avionics, satellite processors, and space-based control systems. Single Event Upsets (SEUs), caused by charged particles striking sensitive nodes in memory cells, can result in bit flips, jeopardizing the integrity of mission-critical operations.

Conventional 6T SRAM cells, though widely used for terrestrial applications, lack the robustness required in aerospace environments due to their limited noise margins and susceptibility to SEU-induced soft errors. This has led to the exploration of radiation-hardened memory cell architectures, with increased transistor redundancy and improved fault-tolerant behavior.

In this context, the 12T SRAM cell design presents a promising solution. By incorporating additional feedback and isolation transistors, the cell improves SEU immunity, read stability, and leakage control. This paper proposes and evaluates a fault-resilient 12T SRAM architecture implemented in nanoscale CMOS technology, emphasizing its suitability for spaceborne systems. The design is simulated under multiple process, voltage, and temperature (PVT) corners and radiation-induced transient faults to validate its performance, stability, and energy efficiency.

I. PROPOSED METHOD

This novel radiation-hardened-by-design (RHBD) 12T storage facility features an easily implementable layout-topology and also takes into consideration the physical mechanism of upset in soft faults. The validation results show that the proposed 12T cell can provide significant radiation resistance. The predicted 12T cell requires more room, energy, and time to read and write than a 13T cell. The 986.2 mV margin of static noise in the hold is more than what a 13T cell can achieve. The error-correcting capabilities of the recommended 12T cell make it more trustworthy. These days, CMOS technology is ubiquitous in the electronics sector. The aircraft industry is another that benefits greatly from CMOS technology. Memories are the primary data storage mechanism in many aeronautical applications. CMOS technology is used in the production of SRAM cells, a kind of memory. The main problem with long-term memory is single-event disruptions (SEUs), which are brought on by particles of radiation. Rising urbanization is directly responsible for the SEUs. As CMOS process technology has advanced, both the critical charge and supply voltage have decreased. A approach free of these SEUs is needed for use in aircraft systems. Where exactly dothey exist in the very radioactive void between the stars? Methods that are radiation- hardened by design (RHBD) that are resistant to soft errors are currently being researched. The primary contribution of this study is a proposal for a low-profile, high-reliability RHBD memory cell.

"Adiabatic logic" refers to low-power electrical circuits that may be employed in either direction. During the adiabatic phase, there is no change in the total quantity of heat or energy in the system, thus the name. Energy dissipation is greatly improved by decreasing circuit size and increasing circuit fineness, which has been a major motivation for studying adiabatic circuits.

A. SCRL NAND

Understanding the big picture behind this group of genes may require dissecting the SCRL NA ND complete loop shown in Figure 1.

This ND uses trapezoidal clocks (Kin1 and / Kin1) to power the top and bottom tracks, rather than the more conventional Vdd and Gne 1. There has been no change to this section. With the exception of P 1, which is connected to Gnd, and /P 1, which is connected to Vdd,

all components are linked to Vdd/2 in the first position, rendering the switch gate superfluous. The transmission gate is turned on once P 1 and P 1 are configured. First steps. Vdd and Gnd are then created from the /first 1 and /first 1 Vdd/2nodes. At this stage, the NA ND of both a and b go through the same non-adiabatic door calculation. Once the output is being utilized by the subsequent gate, the transmitting gate may be gradually disabled. The input may be adjusted and the next phase initiated once the sum of phases 0 and 1 reaches Vdd/2 again. Since a deviation from Vdd/2 would violate the first criterion, a resistor must be disabled and the rails reset to this value.

P-MOS's function when coupled with B input is unclear. Please review the circumstances behind the disappearance of the transistor. Times of the eleventh day.

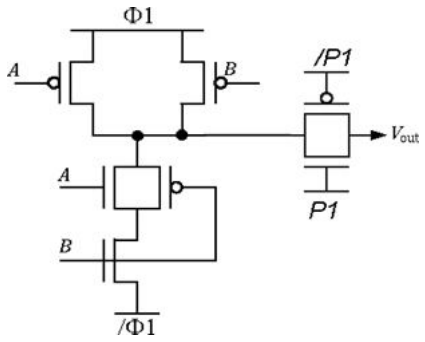


Figure 1 : SCRL NAND

B. 2LAL

Frank's[2] Another significant class of adiabatic circuits is the 2LAL family. This series, like SCRL, has complete plumbing all the way to the gate. Figure 2(a) depicts the fundamental components of 2LAL, a pair of transmission gates used to represent the signals A and A. Because of its simplicity and independence from CMOS, 2LAL is well suited for implementation in cutting-edge devices.

Two transmission gates make up the 2LAL basic buffer feature, seen in Figure 2(b). Each trapezoidal clock's zero point on the fourth cycle happens one and a quarter timeslater than the other. Both vertices start out with a value of 0 at the beginning. If the input is 1, the state will change from 0 to 1 over time. When we go on to "phase 1,"

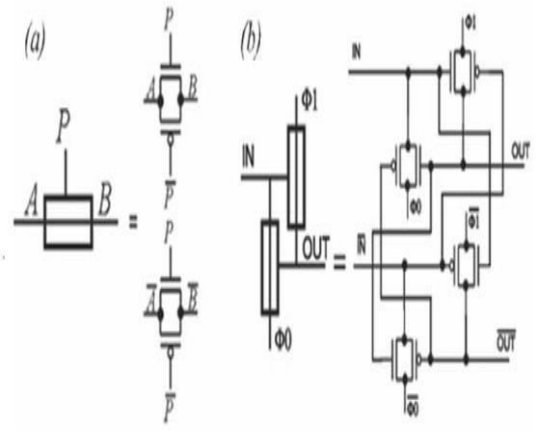
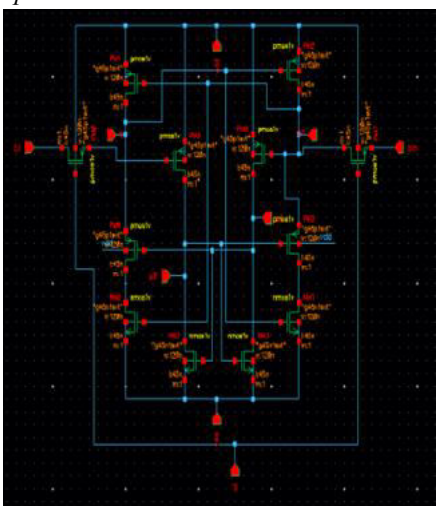


Figure 2: 2LAL Basic Gate(a) and Buffer(b)

When the input is 1, the output and input are both set to 1, and the transistor is disabled to save power. Finally, switch the input back to 0 and keep cycling between 1 and 0. The pipeline is ready to accept a new input after the output passes through the next gate and reverts to 0. 2LAL can build inverters quickly since rails may cross from one portto another.

II. RESULT

A. *Proposed schematic*



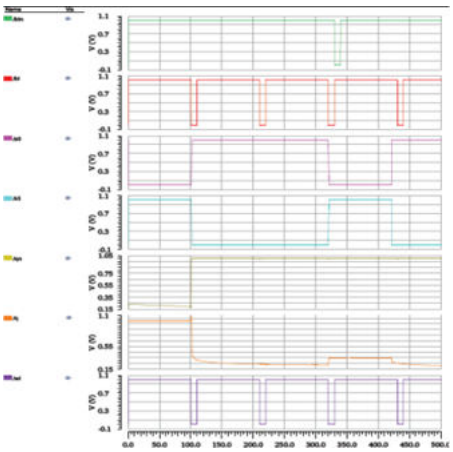


Figure 3: Proposed schematic

Figure 4 : proposed schematic simulation result

A. DELAY

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Parsing                          0.01 seconds
Setup                            0.05 seconds
DC operating point               0.07 seconds
Transient Analysis               0.03 seconds
Overhead                         0.91 seconds
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Total                            1.07 seconds
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A. POWER

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Power Results

VVoltageSource_3 from time 0 to 100
Average power consumed -> 5.594084e-011 watts
Max power 2.061770e+000 at time 8.025e-008
Min power 8.198842e-003 at time 3.20774e-008
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III. CONCLUSION

The proposed fault-resilient 12T SRAM cell offers a compelling memory solution for spaceborne CMOS systems where reliability, data integrity, and radiation tolerance are critical. Through comprehensive simulations and comparative analysis, the design demonstrated significant improvements in SEU resistance, enhanced read and write margins, and robust operation under low supply voltages, outperforming the conventional 6T SRAM cell.

Although the inclusion of extra transistors slightly increases the area, the trade-off is justified by the dramatic gain in reliability and stability, making it ideal for applications in satellite systems, space probes, and aerospace-grade microprocessors. Moreover, the cell's compatibility with standard CMOS technology ensures its adaptability in current semiconductor manufacturing pipelines.

In conclusion, the 12T SRAM architecture represents a viable path forward for radiation-hardened memory design, offering a balance between fault tolerance, low power consumption, and area efficiency. Future work may explore layout-level radiation hardening, adaptive error correction integration, and prototyping the design for field testing in actual aerospace environments.

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